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EXAMINER	
WILLOUGHBY, TERRENCE RONIQUE	
ART UNIT	**PAPER NUMBER**
2836	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/767,045	LOEB ET AL.	
	Examiner	Art Unit	
	Terrence R. Willoughby	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-19,21-67* is/are rejected.

7)☒ Claim(s) *9 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/28/04;5/31/05*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Applicant amendment filed on 4/5/2006 has been entered. Accordingly Claims 1,5,10,12,16,21,26,30,34,36,40,45,49,54,58,62,66 have been amended. No new claims were added. Claims 1-67 remain pending in this application. It also included remarks/arguments.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

3. The drawings are objected to because the resistor in Figure 3 that is connected between the collector of transistor (Q_2) and the power source (V_{DD}) of the biasing network is not labeled. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the

drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3,7,8,10,12-14,18,19,21,23,25-28,30-42,44-49,51,53-56,58,59, 61-64,66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hietala et al. (US 5,150,075) and in view of Bien (US 6,388,525 B1).

Regarding claims 1 and 12, Hietala et al. discloses the claimed said protection circuit for a radio frequency (RF) power amplifier (Fig. 1, 203; column 1, lines 11-12 and column 4, line 23), the RF power amplifier operable to receive an RF input signal (Fig. 1, 209) and amplify the RF input signal (column 4, lines 25-30), the protection circuit comprising: the control circuitry including ramp circuitry (column 1, lines 1-3).

Hietala et al. does not disclose a shunt circuitry or a shunt switch operable to shunt an RF input signal to AC ground and release the RF input signal from AC ground.

However, Bien discloses a variable gain control circuit including shunt circuitry (column 3, lines 6-10) operable to shunt an RF input signal to AC ground (Fig. 1, Zs; column 3, lines 17-20; column 4, line 5), the shunt circuitry including a shunt switch (Fig. 7, M21; and column 4, lines 58-59 and column 7, lines 40-43) operable to shunt an RF input signal (column 1, lines 52-55 and column 4, line 5) to AC ground.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have combine the power amplifier protection circuit taught by Hietala et al. to the variable gain control circuit of Bien for the purpose of transmitting and receiving extremes signals more reliably without adding excessive noise with the variable attenuation devices built into the amplifier circuit. In such a configuration of the above mentioned combination the shunt switch will release the RF input signal from AC ground for input to an RF amplifier. The shunt switch would be controlled by control circuitry and the ramp circuitry would be operable to control the shunt switch so that the shunt switch releases the RF signal from AC ground for input to an RF amplifier as required by the claim.

Regarding claims 2 and 13, Hietala et al. in view of Bien discloses the claimed said protection circuit of claims 1 and 12 above, wherein an linear region MOSFET (Bien, abstract, line 1; column 7, line 49-51; Fig. 7, M21).

Regarding claims 3 and 14, Hietala et al. in view of Bien discloses the claimed said protection circuit of claims 2 and 13 above, wherein the shunt switch comprises a linear region MOSFET is a NMOS transistor (Bien, abstract, line 1; column 7, line 49; Fig. 7, M21).

Regarding claims 7 and 18, Hietala et al. in view of Bien discloses the claimed said protection circuit of claims 1 and 12 above, further comprising bias shutdown circuitry operable to shut off a bias voltage (Bien, column 7, line 7) or a bias current (Bien, column 7, line 4) being supplied to an output transistor (Bien, Fig. 7, Qo and column 7, line 15-16) of the RF power amplifier (Bien, column 1, lines 52-55 and column 1, line 45).

Regarding claims 8 and 19, Hietala et al. in view of Bien discloses the claimed said protection circuit of claims 7 and 18 above, further comprising peak detection circuitry (Hietala et al., Fig. 2,211 and abstract, lines 4-10) operable to monitor an output voltage of the RF amplifier and provide a protection signal (Hietala, column 6, lines 10-17) to the shunt circuitry (Bien, column 3, lines 6-10) and the bias shutdown circuitry

(Bien, column 7, lines 4-15) when the output voltage of the RF amplifier exceeds a threshold voltage level(Hietala et al., abstract, lines 8-10).

Regarding claims 10 and 21, Hietala et al. in view of Bien discloses the claimed said protection circuit of claims 1 and 12 above, wherein the control circuitry (Hietala et al., column 1, lines 1-3) further includes a delay circuit (Hietala et al., column 6, lines 18-21) operable to delay the ramp control circuitry from releasing the RF input signal from AC ground.

Regarding claim 23, Hietala et al. in view of Bien discloses the claimed said RF power amplifier (Hietala et al., column 1, lines 11-12), comprising: amplifier circuitry operable to amplify an RF input signal and provide an amplified RF output signal (Hietala et al., column 4, lines 23-68 and column 5, lines 1-5); peak detection circuitry (Hietala et al., Fig. 2, 211 and abstract, lines 4-10) operable to monitor the amplified output RF signal and detect when the amplified output signal exceeds a threshold voltage level (Hietala et al., abstract, line 8-10); and a bias network (Bien, column 7, lines 4-15) operable to provide a bias to the amplifier circuitry and shut off the bias to the amplifier circuitry when the peak detection circuitry (Hietala et al., Fig. 2, 211 and abstract, lines 4-10) detects that the amplified output signal has exceeded the threshold voltage level.

Regarding claim 25, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 23 above, further comprising shunt circuitry (Bien, column 3, lines 6-10) operable to shunt the RF input signal to AC ground (Bien, Fig. 1, Zs, column 3, lines 17-20 and column 4, line 5) when the peak detection circuitry (Hietala et al., Fig. 2,211 and abstract, lines 4-10) detects that the amplified output signal has exceeded the threshold voltage level (Hietala, abstract line 8-10).

Regarding claim 26, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 25 above, wherein the shunt circuitry comprises: a shunt switch (Bien, Fig. 7, M21; column 7, lines 40-43) operable to shunt the RF input signal to AC ground and release the RF input signal from AC ground (Bien, Fig. 1, Zs, column 3, lines 17-20 and column 4, line 5), the shunt switch being control by control circuitry including ramp circuitry (Hietala et al., column 1, lines 1-3), the ramp circuitry operable to control the shunt switch so that the shunt switch releases the RF signal from AC ground for input to an RF amplifier.

Regarding claim 27, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 26 above, wherein the shunt switch comprises a linear region MOSFET (Bien, abstract, line 1; column 7, line 49; Fig. 7, M21).

Regarding claim 28, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 27 above, wherein the linear region MOSFET is an NMOS transistor (Bien, abstract, line 1; column 7, line 49; Fig. 7, M21).

Regarding claim 30, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 26 above, further includes delay circuitry (Hietala et al., column 6, lines 18-21) operable to delay the ramp control circuitry from releasing the RF input signal from AC ground (Hietala et al., column 6, lines 44-47).

Regarding claim 31, Hietala et al. in view of Bien discloses the claimed method for protecting an RF power amplifier from elevated output voltages, the method comprising: detecting (Hietala et al., Fig. 2,211) an output voltage of an RF power amplifier exceeding a threshold voltage level (Hietala et al., abstract, lines 8-10); shutting off bias to an outputs transistor (Bien, column 7, line 4-18) of the RF power amplifier (Bien, column 1,lines 52-55 and column 1, line 45) when the output voltage exceeds the threshold voltage level; and turning off the output transistor of the RF power amplifier when the output voltage exceeds the threshold voltage level (Hietala et al., Fig. 2, 211 and abstract, lines 8-10).

Regarding claim 32, Hietal et al. in view of Bien discloses the claimed said method of claim 31 above, further comprising: shunting an RF input signal (Bien, column 3, lines 6-10) to the RF power amplifier to AC ground (Bien, Fig. 1, Zs; column

3, lines 17-20; column 4, line 5) when the output voltage exceeds the threshold voltage level (Bien, column 7, lines 4-15).

Regarding claim 33, Hietal et al. in view of Bien discloses the claimed said method of claim 32 above, further comprising: supplying bias to the output transistor and turning on the output transistor when the output voltage is reduced to a level below the threshold voltage level.

Regarding claim 34, Hietal et al. in view of Bien discloses the claimed said method of claim 33 above, further comprising: releasing the RF input signal from AC ground when the output voltage is reduced to a level below the threshold voltage level.

Regarding claim 35, Hietal et al. in view of Bien discloses the claimed said method of claim 34 above, further comprising: delaying the gradual release of the RF input signal from AC ground until a time after the output transistor has turned on.

Regarding claim 36, Hietal et al. in view of Bien discloses the claimed said method of claim 32 above, further comprising providing an asymmetrical control that quickly shuts off the power amplifier and turns on the power amplifier at a gradual rate.

Regarding claim 37, Hietal et al. in view of Bien discloses the claimed said protection circuit comprising: means for detecting (Hietala et al., Fig. 2, 211 and

abstract, lines 4-10) an output voltage of an RF power amplifier exceeding a threshold voltage level;(Hietala et al., abstract, lines 8-10) means for shutting off bias to an output transistor of the RF power amplifier when the output voltage exceeds the threshold voltage level (Bien, column 7, lines 4-18; and means for turning off the output transistor of the RF power amplifier when the output voltage exceeds the threshold voltage level(Bien, column 7,lines 4-18).

Regarding claim 38, Hietal et al. in view of Bien discloses the claimed said protection circuit of claim 37 above, further comprising: means for shunting an RF input signal to the RF power amplifier to AC ground when the output voltage exceeds the threshold voltage level (Bien, Fig. 1, Zs; column 3, lines 17-20; column 4, line 5).

Regarding claim 39, Hietala et al. in view of Bien discloses the claimed said protection circuit of claim 38 above, further comprising: means for supplying bias to the output transistor and means for turning on the output transistor (Bien, column 7, 4-15).

Regarding claim 40, Hietala et al. in view of Bien discloses the claimed said protection circuit of claim 39 above, further comprising: means for releasing (Hietala et al., column 2, lines 10-20) the RF input signal from AC ground when the output voltage is reduced to a level below the threshold voltage level (Hietala et al., abstract, lines 8-10).

Regarding claim 41, Hietala et al. in view of Bien discloses the claimed said protection circuit of claim 40 above, further comprising: means for delaying (Hietala et al., column 6, lines 18-21) the gradual release of the RF input signal from AC ground until a time after the output transistor has turned on.

Regarding claim 42, Hietala et al. in view of Bien discloses the claimed said RF power amplifier (Hietala et al., column 1, lines 11-12) operable to amplify an RF input signal, the RF power amplifier including, amplifier circuitry (Hietala et al., Fig. 2) operable to amplify the RF input signal and provide an amplified RF output signal (Hietala et al., column 4, lines 23-68 and column 5, lines 1-5); peak detection circuitry (Hietala et al., Fig. 2, 211 and abstract, lines 4-10) operable to monitor the amplified output RF signal and detect when the amplified output signal exceeds a threshold voltage level; and a bias network(Bien, column 7, lines 4-15) operable to provide a bias to the amplifier circuitry and shut off the bias to the amplifier circuitry when the peak detection circuitry detects(Hietala et al., Fig. 2, 211 and abstract, lines 4-10) that the amplified output signal has exceeded the threshold voltage level.

Regarding claim 44, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 42 above, further comprises shunt circuitry (Bien, column 3, lines 6-10) operable to shunt the RF input signal to AC ground (Bien, Fig. 1, Zs; column 3, lines 17-20; column 4, line 5) when the peak detection circuitry (Hietala et al., Fig. 2,

211 and abstract, lines 4-10) detects that the amplified output signal has exceeded the threshold voltage level (Bien, column 7, lines 4-15).

Regarding claim 45, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 44 above, wherein the shunt circuitry (Bien, column 3, lines 6-10) comprises: a shunt switch (Bien, Fig. 7, M21; column 7, lines 40-43) operable to shunt the RF input signal to from AC ground (Bien, Fig. 1, Zs and column 3, lines 17-20), the AC ground and release the RF input signal shunt switch being controlled by control circuitry; and the control circuitry including ramp circuitry (Hietala, column 1, lines 1-3), the ramp circuitry operable to control the shunt switch so that the shunt switch releases the RF signal from AC ground for input to an RF amplifier.

Regarding claim 46, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 45 above, wherein the shunt switch comprises a linear region MOSFET (Bien, abstract, line 1; column 7, line 49; Fig.7, M21).

Regarding claim 47, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 46 above, wherein the linear region MOSFET is an NMOS transistor (Bien, abstract, line 1;column 7,line 49; Fig. 7, M21).

Regarding claim 49, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 45 above, wherein the control circuitry (Hietala et al., column

1, lines 1-3) further includes delay circuitry (Hietala et al., column 6, lines 18-21) operable to delay the ramp çontrol circuitry from releasing the RF input signal from AC ground.

Regarding claims 42, 44-47,49, It would have been obvious to one of ordinary skill in the art at the time the invention was made that the RF power amplifier claimed above was designed to be implemented in a wireless transceiver as both references teach the use of power amplifiers in radio telecommunication systems.

Regarding claim 51, Hietala et al. in view of Bien discloses the claimed said RF power amplifier, comprising: amplifying means (Hietala et al., column 1, lines 11-12) for amplifying an RF input signal and providing an amplified RF output signal (Hietala et al., column 4, lines 23-68 and column 5, lines 1-5); detecting means (Hietala et al., Fig. 2, 211 and abstract, lines 4-10) for monitoring the amplified output RF signal and detecting when the amplified output signal exceeds a threshold voltage level; and biasing means(Bien, column 7, lines 4-15) for providing a bias means and shutting off the bias to the amplifying means when the detecting means (Hietala et al., Fig. 2, 211 abstract, lines 4-10) detects that the amplified output signal has exceeded the threshold voltage level.

Regarding claim 53, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 51 above, further comprising shunting means (Bien, column 3,

lines 6-10) for shunting the RF input signal to AC ground (Bien, column 7, lines 40-43) when the detecting means (Hietala et al., Fig. 2, 211 and abstract, lines 4-10) detects that the amplified output signal has exceeded the threshold voltage level.

Regarding claim 54, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 53 above, wherein the shunting means (Bien, column 1, lines 52-55) comprises: switching means for shunting the RF input signal to AC ground (Bien, Fig. 1, Zs; column 3, lines 17-20 and column 4,1ine 5) and releasing the RF input signal from AC ground, the switching means (Bien, Fig. 7, M21; column 7,lines 40-43) being controlled by control circuitry; and the control circuitry (Hietala et al., column 1, lines 1-3) including ramping means for controlling the switching means so that the switching means releases the RF signal from AC ground for input to an RF amplifier.

Regarding claim 55, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 54 above, wherein the switching means comprises a linear region MOSFET (Bien, abstract, line 1; column 7,line 49; Fig. 7, M21).

Regarding claim 56, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 55 above, wherein the linear region MOSFET is an NMOS transistor (Bien, abstract, line 1; column 7,line 49; Fig. 7, M21).

Regarding claim 58, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 54 above, wherein the control circuitry (Hietala et al., column 1, lines 1-3) further includes delaying means (Hietala et al., column 6, lines 18-21) for delaying the ramping means from releasing the RF input signal from AC ground (Hietala et al., column 6, lines 44-47).

Regarding claim 59, Hietala et al. in view of Bien discloses the claimed said RF power amplifier operable to amplify an RF input signal, the RF power amplifier including, amplifying means (Hietala et al., column 1, lines 11-12) for amplifying an RF input signal and provide an amplified RF output signal (Hietala et al., column 4, lines 23-68 and column 5, lines 1-5); detecting means (Hietala et al., Fig. 2, 211 and abstract, lines 4-10) for monitoring the amplified output RF signal and detecting when the amplified output signal exceeds a threshold voltage level; and biasing means(Bien, column 7, lines 4-15) for providing a bias means and shutting off the bias to the amplifying means when the detecting means (Hietala et al., Fig. 2, 211 abstract, lines 4-10) detects that the amplified output signal has exceeded the threshold voltage level.

Regarding claim 61, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 59 above, further comprising shunting means (Bien, column 3, lines 6-10) for shunting the RF input signal to AC ground (Bien, column 7, lines 40-43) when the detecting means (Hietala et al., Fig. 2, 211 and abstract, lines 4-10) detects that the amplified output signal has exceeded the threshold voltage level.

Regarding claim 62, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 61 above, wherein the shunting means (Bien, column 1, lines 52-55) comprises: switching means for shunting the RF input signal to AC ground (Bien, Fig. 1, Zs; column 3, lines 17-20 and column 4,1ine 5) and releasing the RF input signal from AC ground, the switching means (Bien, Fig. 7, M21; column 7,lines 40-43) being controlled by control circuitry; and the control circuitry (Hietala et al., column 1, lines 1-3) including ramping means for controlling the switching means so that the switching means releases the RF signal from AC ground for input to an RF amplifier.

Regarding claim 63, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 62 above, wherein the switching means comprises a linear region MOSFET (Bien, abstract, line 1; column 7,line 49; Fig. 7, M21).

Regarding claim 64, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 63 above, wherein the linear region MOSFET is an NMOS transistor (Bien, abstract, line 1; column 7,line 49; Fig. 7, M21).

Regarding claim 66, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 62 above, wherein the control circuitry (Hietala et al., column 1, lines 1-3) further includes delaying means (Hietala et al., column 6, lines 18-21) for

delaying the ramping means from releasing the RF input signal from AC ground (Hietala et al., column 6, lines 44-47).

Regarding claims 59-66, It would have been obvious to one of ordinary skill in the art at the time the invention was made that the RF power amplifier claimed above was designed to be implemented in a wireless transceiver.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 23,24,31,37,42,43,50,51,52,59,60,67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Denning et al. (US 6,720,831 B2).

Regarding claim 23, Denning et al. discloses a RF power amplifier (Fig. 1,12) comprising: amplifier circuitry operable to amplify an RF input signal and provide an amplified RF output signal (column 3, lines 2-3); peak detection circuitry (Fig. 1,14) operable to monitor the amplified output RF signal and detect when the amplified output signal exceeds a threshold voltage level (column 3, lines 25-27); and a bias network (Fig. 1,18) operable to provide a bias to the amplifier circuitry and shutoff the

bias to the amplifier circuitry when the peak detection circuitry detects that the amplified output signal has exceeded the threshold voltage (column 2, lines 5-13).

Denning et al. discloses a processing circuit (Fig. 1, 16) may be operable to provide different biasing circuits for power amplifiers. (See Fig. 2A and Fig. 2B and column 4, lines 27-32 and column 4, lines 41-43). Denning et al. also discloses that the bias current can be shut off by the current mirror when the sensing circuit detects an output over the threshold voltage level (column 2, lines 5-13).

Regarding claims 24 and 37, Denning et al. discloses a RF power amplifier (Fig. 1, 12) of claim 23, wherein the bias network (Fig. 1, 18) is operable to further turn off an output transistor (column 1, lines 35-38) of the amplifier circuitry when the peak detection circuitry detects that the amplified output signal has exceeded the threshold voltage level (column 1, lines 65-67 and column 2, lines 1-13).

Regarding claim 31, one would necessarily perform the recited method steps in using the RF power amplifier rejected above in claims 23-24.

Regarding claims 42,43,51,52,59,60, please see the above rejection of claims 23 and 24 in regards to the claimed limitations. It would have been obvious to one of ordinary skill in the art at the time the invention was made that the RF power amplifier

claimed above was designed to be implemented in a wireless transceiver. Denning teaches that the power amplifier is used in wireless communication applications.

Regarding claim 50, please see the above rejection of claim 42 in regards to the claimed limitations. It would have been obvious to one of ordinary skill in the art at the time the invention was made that in wireless technologies, the IEEE standards mentioned in the claim are necessarily met by standard wireless transceivers to enable the transceiver to operate and comply in conjunction with the safety and operational requirements.

Regarding claim 67, please see the above rejection of claim 59 in regards to the claimed limitations. It would have been obvious to one of ordinary skill in the art at the time the invention was made that in wireless technologies, the IEEE standards mentioned in the claim are necessarily met by standard transceivers to enable the transceivers to operate and comply in conjunction with the safety and operational requirements.

8. Claims, 4-6,11,15-17,22,29,48,57, 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hietala et al. (US 5,150,075) and in view of Bien (US 6,388,525) and in further view of Macphail et al. (US 6,603,335).

Regarding claims 4 and 15, Hietala et al. in view of Bien discloses the claimed said protection circuit of claims 1 and 12 above, comprising a ramp circuit, however they both do not disclose an RC network.

However, Macphail et al. discloses a ramp circuit for a power amplifier (Fig. 1) that includes a RC network (column 3, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ramping circuit of Hietala et al. and Bien by providing a RC network taught by Macphail et al. for controlling the output of the power amplifier by ramping up the amplifier output power to its proper frequency therefore to transmit the desired data at the output power level, and ramping down its power amplifier so as not to disturb or interfere with the other cellular telephone users sharing the same frequency or wireless channels.

Regarding claims 5 and 16, Hietala et al. in view of Bien and further view of Macphail et al. discloses the claimed said protection circuit of claims 4 and 15 above, wherein the shunt switch (Bien, Fig. 7, M21; column 7, lines 40-43) gradually releases the RF signal from AC ground exponentially (Maephail et al., column 4, lines 15-17). It would have been obvious to those skilled in the art at the time of the invention was made that the normal operation of any device connected to a ramp circuit that includes

an RC network wherein the shunt switch release the RF signal from AC ground exponentially.

Regarding claims 6 and 17, Hietala et al. in view of Bien and further view of Macphail et al. discloses the claimed said protection circuit of claims 4 and 15 above, wherein the ramp circuitry releases in accordance with a discharge of a capacitor in the RC network (Machphail, column 5, lines 24-26).

Regarding claims 11 and 22, Hietala et al. in view of Bien and further view of Macphail et al. discloses the protection circuit of claims 10 and 21 above, wherein the delay circuitry includes an RC network (Machphail, column 1, lines 62-64; column 2, lines 49-51).

Regarding claim 29, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 26 above, including a ramp circuitry, however they both do not disclose a RC network.

However, Macphail et al. discloses a ramp circuit for a power amplifier (Fig. 1) that includes a RC network (column 2, lines 49-51 and column 3, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ramp circuitry of Hietala et al. and Bien by

providing a RC network taught by Macphail et al. for controlling the output of the power amplifier by ramping up the amplifier output power to its proper frequency therefore to transmit the desired data at the output power level and ramping down its power amplifier so as not to disturb or interfere with the other cellular telephone users sharing the same frequency or wireless channels.

Regarding claim 48, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 45 above, with a ramp circuitry, however they both do not disclose a RC network.

However, Macphail et al. discloses a ramp circuit for a power amplifier (Fig. 1) that includes a RC network (column 2, lines 49-51 and column 3, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ramp circuitry of Hietala et al. and Bien by providing a RC network taught by Macphail et al. for controlling the output of the power amplifier by ramping up the amplifier output power to its proper frequency there to transmit the desired data at the output power level and ramping down its power amplifier so as not to disturb or interfere with the other cellular telephone users sharing the same frequency or wireless channels.

Regarding claim 48, it would been obvious to those skilled in the art at the time the invention was made that the RF power amplifier claimed above was designed to be implemented in a wireless transceiver.

Regarding claim 57, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 54 above, with a ramping means, however they both do not disclose a RC network.

However, Macphail et al. discloses a ramp circuit for a power amplifier (Fig. 1) that includes a RC network (column 2, lines 49-51 and column 3, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ramp circuitry of Hietala et al. and Bien by providing a RC network taught by Macphail et al. for controlling the output of the power amplifier by ramping up the amplifier output power to its proper frequency therefore to transmit the desired data at the output power level and ramping down its power amplifier so as not to disturb or interfere with the other cellular telephone users sharing the same frequency or wireless channels.

Regarding claim 65, Hietala et al. in view of Bien discloses the claimed said RF power amplifier of claim 62 above, including a ramp circuitry, however they both do not disclose a RC network.

However, Macphail et al. discloses a ramp circuit for a power amplifier (Fig. 1) that includes a RC network (column 2, lines 49-51 and column 3, lines 50-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the ramp circuitry of Hietala et al. and Bien by providing a RC network taught by Macphail et al. for controlling the output of the power amplifier by ramping up the amplifier output power to its proper frequency therefore to transmit the desired data at the output power level and ramping down its power amplifier so as not to disturb or interfere with the other cellular telephone users sharing the same frequency or wireless channels.

Allowable Subject Matter

9. Claims 9 and 20 are objected to as being dependent upon a rejected base claim 8 and 19, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Combined claims 9 and 20 would be allowable over the art of record because the prior art does not teach a programmable peak detection circuit as set forth in the claimed invention.

Response to Arguments

10. In response to Applicant's arguments with respect to Claims 23, 24, 31, 37,42,43,50,51,52,59,60,67 have been considered but are moot in view of the new ground(s) of rejection.

11. In response to Applicant's arguments with respect to Claims 1-3,7,8,10,12-14,18,19,21,23,25-28,30-42,44-49,51,53-56,58,59, 61-64,66 have been fully considered but are not persuasive.

12. The Examiner disagrees with the Applicants assessment in response to Claim 1, that Bien's " circuitry is configured once, to set gain for the circuitry and is not operable to shunt an RF signal to AC ground".

Bien discloses an amplifier with a controllable variable signal gain (abstract) configured to set the gain depending upon the desired controlling effect, to produce a number of different control voltage versus the input signal voltage or gain profiles (Fig. 6 and column 6, lines 57-65). Further, Bien discloses a shunt impedance circuit (column 3, lines 6-10) operable to shunt an RF input signal to AC ground (Fig. 1, Zs; and column 3, lines 17-20 and column 4, line 5), the shunt circuitry including a shunt switch (column 1, lines 52-55; column 4, lines 20-21 and column 4, line 5) to AC ground. As indicated in column 4, see the reference Table. Bien discloses the shunt impendence (Zs) shunting a RF input signal to AC ground when the shunt impedance (Zs) having zero (ohms) will introduce infinite attenuation (dB) indicating the input signal of the amplifier is short-

circuited to ground and vice versa when the shunt impedance (Zs) having an infinite (ohms) will introduce zero attenuation (0.0) indicating that the input signal of the amplifier is released from ground.

Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replace the shunt impedance (Zs) variable resistance with any type of shunt switch, which is well known in the art to use a shunting switch to turn on and off a the device based on the desired attenuation range and since the designer has the opportunity to pick the right configuration required by the features/ design specifications of the rest of the circuit as a whole.

13. The Examiner also disagrees with the Applicant's assessment in response to Claim 23, that Bien " has no bias circuit operable to shut off the bias to the amplifier".

However, Bien discloses a bias voltage and bias current for the amplifier formed by transistor (Qo) that is operable to turned off or on (column 7, lines 4-15), and could be read on the "the bias circuit operable to shut off the bias to the amplifier" in the claims.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Black et al. (US 6,169,886 B1) discloses a power amplifier of communication devices, to facilitating control of such power amplifiers according to a delayed waveform. Arnott (US 2003/0045251 A1) discloses a power amplifier overload protection, upon detection of an overload, steps are taken to shunt the RF drive or

reduce bias at one or more preceding stages of the amplifier to limit the excessive voltage or current in the output stage.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terrence R. Willoughby whose telephone number is 571-272-2725. The examiner can normally be reached on 8-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800 ext. 36. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRW
6/26/06

Stephen W Jackson
6-26-06

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PRIMARY EXAMINER